Modeling of Noise Parameters of MESFET's and MODFET's and Their Frequency and Temperature Dependence

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Abstract —A simple noise model of a microwave MESFET (MODFET, HEMT, etc.) is described and verified at room and cryogenic temperatures. Closed-form expressions for $T_{\min}$, the minimum noise temperature, $Z_{g\,\mathrm{opt}}$, the optimum generator impedance, g_n, the noise conductance, and $Z^M_{g\,\mathrm{opt}}$, the generator impedance minimizing noise measure, are given in terms of the frequency, the elements of a FET equivalent circuit, and the equivalent temperatures of intrinsic gate resistance and drain conductance to be determined from noise measurement. These equivalent temperatures are demonstrated in the example of a Fujitsu FHR01FH MODFET to be independent of frequency in the frequency range in which $1/f$ noise is negligible. Thus, the model allows prediction of noise parameters for a broad frequency range from a single-frequency noise parameters measurement. The relations between this approach and other relevant studies are established.

I. Introduction

THE NOISE performance of field-effect transistors (FET's) has been a subject of study for more than a quarter of a century [1]–[20]. It remains a subject of active research [18]–[20], as MODFET's (HEMT's) continue to set records for noise performance at both room and cryogenic temperatures (for example, [22]–[26]). In spite of a considerable effort in this field, a noise model which could be helpful in understanding noise sources within a MESFET (MODFET, HEMT) and at the same time be useful in a circuit design has not really emerged.

The published studies of noise properties of FET's may be divided into two distinctive groups. The first group, as a starting point of analysis, considers fundamental equations of transport in semiconductors [1]–[11]. Most papers in this category published over the years may be viewed as progressively more sophisticated treatments of the problem originally tackled by Van der Ziel [1], [2]. Ultimately, a full Monte Carlo particle study of the noise figure of FET's was proposed [11]. Although a MOSFET wafer structure is different than that of a MESFET, the methods employed in noise studies are basically the same [8], [10], [20] as those applied to FET's [5], [9], [20].

The second group of published studies [12]–[19] addresses the issue of what needs to be known about the device in addition to its equivalent circuit to predict the noise performance. Most often used is the semiempirical approach originated by Fukui [12]–[16], in which relations between the minimum noise figure at a given frequency and the values of transconductance, g_m, gate to source capacitance, C_{gs}, and source and gate resistances, r_s and r_g, are established. A quantitative agreement may be obtained only after the proper choice of a fitting factor [12], [13], [15] or fitting factors [16]. The extension of this approach to other noise parameters [12] results quite often in a nonphysical two-port [14]. The Fukui approach, although very widely used by device technologists, does not provide any insight into the nature of a noise-generating mechanism in a FET as the fitting factors do not possess physical meaning.

The most comprehensive treatment of the signal and noise properties of a MESFET is that published by Pucel *et al.* [5]. It calls for three frequency-independent noise coefficients to be known in addition to small-signal parameters of an intrinsic FET in order to determine four noise parameters at any given frequency. Recent work by Gupta *et al.* [18], [19], however, claims a good agreement over a wide frequency range between measured noise parameters and those predicted from the knowledge of an equivalent circuit and a single frequency-independent constant.

The method presented in this paper uses simple circuit theory arguments to show that for an intrinsic device two frequency-independent constants (equivalent temperatures of the intrinsic gate resistance and drain conductance) need to be known, in addition to the elements of an equivalent circuit, to predict all four noise parameters at any frequency. These constants in the experimental example of a Fujitsu FHR01FH HEMT are frequency independent in the frequency range in which $1/f$ noise is negligible. Surprisingly, it is also demonstrated that at both room and cryogenic temperatures the effective gate temperature is within measurement errors equal to the ambient temperature of the device, thus corroborating the room-temperature results of Gupta *et al.* [18], [19].

The second section of this paper presents the derivation of expressions for the noise parameters of an intrinsic FET. The proposed model is then applied to the analysis of the noise performance of a FHR01FH HEMT at both

Manuscript received July 12, 1988; revised April 27, 1989.
The author is with the National Radio Astronomy Observatory Charlottesville, VA 22903. The observatory is operated by Associated Universities, Inc., under contract with the National Science Foundation.
IEEE Log Number 8929181.

0018-9480/89/0900-1340$01.00

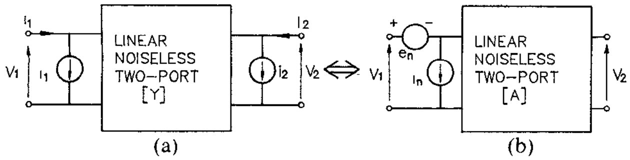


Fig. 1. Noise representation in linear two-ports: (a) involving current noise sources at the input and output and (b) involving current and voltage noise source at the input.

room and cryogenic temperatures in Section III, and the results are discussed in Section IV. Finally, comparisons with other models are offered in Section V.

II. Noise Parameters of FET Chip

A. Representation of Noise in Two-Ports

Three representations of noise in a linear two-port are used in this paper. The representation in Fig. 1(a) is natural for the admittance representation of signal properties of a two-port, and the corresponding noise parameters are [28] (refer to Fig. 1)

$$G_1 = \frac{\overline{|i_1|^2}}{4kT_0\,\Delta f} \qquad G_2 = \frac{\overline{|i_2|^2}}{4kT_0\,\Delta f}$$

$$\rho_c = \frac{\overline{i_1^* i_2}}{\sqrt{\overline{|i_1|^2}\,\overline{|i_2|^2}}} \tag{1}$$

where k is Boltzmann's constant, T_0 is the standard temperature of 290 K, and Δf is the incremental bandwidth. The representation in Fig. 1(b) is natural for *ABCD* matrix representation, and the corresponding noise parameters are [28]

$$R_n = \frac{\overline{|e_n|^2}}{4kT_0\,\Delta f} \qquad g_n = \frac{\overline{|i_n|^2}}{4kT_0\,\Delta f}$$

$$\rho = \frac{\overline{e_n^* i_n}}{\sqrt{\overline{|e_n|^2}\,\overline{|i_n|^2}}}. \tag{2}$$

The third representation, consisting of minimum noise temperature, $T_{\min}$, optimal source impedance, $Z_{\text{opt}} = R_{\text{opt}} + jX_{\text{opt}}$, and noise conductance, g_n or parameter $N = R_{\text{opt}} g_n$ (as defined by Lange [32]), has been found particularly useful in describing the noise parameters of a FET. In this representation, the expressions for noise temperature, T_n, and noise measure M of a two-port driven by generator impedance Z_g are

$$T_n = T_{\min} + T_0 \frac{g_n}{R_g} |Z_g - Z_{\text{opt}}|^2$$

$$= T_{\min} + NT_0 \frac{|Z_g - Z_{\text{opt}}|^2}{R_g R_{\text{opt}}} \tag{3}$$

$$T_n = T_{\min} + 4NT_0 \frac{|\Gamma_g - \Gamma_{\text{opt}}|^2}{\left(1 - |\Gamma_{\text{opt}}|^2\right)\left(1 - |\Gamma_g|^2\right)} \tag{4}$$

$$M = \frac{T_n}{T_0} \frac{1}{1 - \dfrac{1}{G_a}} \tag{5}$$

where

$$\Gamma_{\text{opt}} = \frac{Z_{\text{opt}} - Z_0}{Z_{\text{opt}} + Z_0}$$

Z_0 is a reference impedance, and G_a is available gain. $T_{\min}$ and N remain invariant if a lossless reciprocal two-port is connected to the input (and/or output) of a noisy two-port [32]. The minimum value of noise measure, $M_{\min}$, which occurs for certain generator impedance $Z_{\text{opt}}^M \neq Z_{\text{opt}}$ is invariant upon arbitrary linear lossless embedding [36], [37]. Also, for $T_{\min}$ and N to represent a physical two-port, the following inequality has to be satisfied [14], [27], [33]:

$$T_{\min} \leqslant 4NT_0. \tag{6}$$

B. Noise Parameters of a FET Chip

An equivalent circuit of a FET chip is shown in Fig. 2. Parasitic resistances contribute only thermal noise and with a knowledge of the ambient temperature, T_a, their influence can be easily taken into account. In fact, an arbitrary lossy reciprocal two-port at the input and/or output and/or in a feedback path can be easily de-embedded using formulas of [34] and [35]. The noise properties of an intrinsic chip are then treated by assigning equivalent temperature T_g and T_d to the remaining resistive (frequency-independent) elements of the equivalent circuit r_{gs} and g_{ds}, respectively. No correlation is assumed between the noise sources represented by the equivalent temperatures T_g and T_d. This yields a noise equivalent network for an intrinsic chip shown in Fig. 3.

Straightforward comparison of the equivalent networks of Fig. 1(a) and Fig. 3 and the use of definitions (1) give

$$G_1 = \frac{T_g}{T_0} \frac{r_{gs}(\omega C_{gs})^2}{1 + \omega^2 C_{gs}^2 r_{gs}^2} \tag{7}$$

$$G_2 = \frac{T_g}{T_0} \frac{g_m^2 r_{gs}}{1 + \omega^2 C_{gs}^2 r_{gs}^2} + \frac{T_d}{T_0} g_{ds} \tag{8}$$

$$\text{cor}_c = \rho_c \sqrt{G_1 G_2} = \frac{-j\omega g_m C_{gs} r_{gs}}{1 + \omega^2 C_{gs}^2 r_{gs}} \frac{T_g}{T_0}. \tag{9}$$

It should be stressed that the noise representation of Fig. 1(a) is used as an intermediate step in all previous analyses, which lead to the determination of four noise parameters [5], [8]–[10]. Comparison with Pucel *et al.* [5] shows $\rho_c = -jC$. Assuming $T_d = 0$ in (8) gives $\rho_c = -j1$. That is, the noise voltage source $\overline{e_{gs}^2}$ (Fig. 3) models a noise process which produces perfectly correlated noise currents in drain and gate with a purely imaginary correlation coefficient. The current noise source $\overline{i_{ds}^2}$ models a noise process which produces noise current only in a drain circuit.

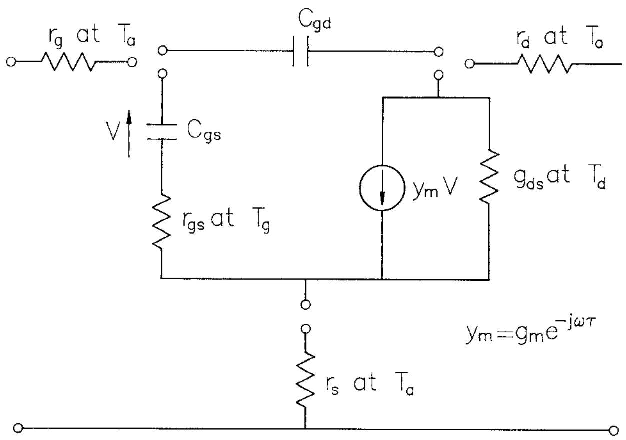


Fig. 2. Equivalent circuit of FET (HEMT, MODFET) chip. Noise properties of an intrinsic chip are represented by equivalent temperatures: T_g of r_{gs}, and T_d of g_{ds}. Noise contribution of ohmic resistances r_s, r_g, and r_d are determined by physical temperature T_a of a chip. The process of de-embedding is illustrated by unconnected elements (compare Table I).

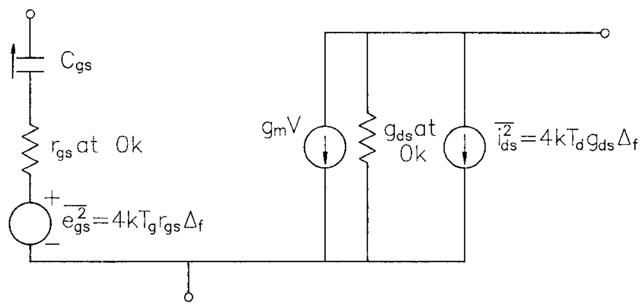


Fig. 3. Noise equivalent circuit of an intrinsic chip.

The noise parameters for the other two representations defined in subsection II-A can be found to be

$$X_{\text{opt}} = \frac{1}{\omega C_{gs}} \tag{10}$$

$$R_{\text{opt}} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{r_{gs}}{g_{ds}} \frac{T_g}{T_d} + r_{gs}^2} \tag{11}$$

$$T_{\min} = 2\frac{f}{f_T}\sqrt{g_{ds} r_{gs} T_g T_d + \left(\frac{f}{f_T}\right)^2 r_{gs}^2 g_{ds}^2 T_d^2} + 2\left(\frac{f}{f_T}\right)^2 r_{gs} g_{ds} T_d \tag{12}$$

$$g_n = \left(\frac{f}{f_T}\right)^2 \frac{g_{ds} T_d}{T_0} \tag{13}$$

$$\frac{4NT_0}{T_{\min}} = \frac{2}{1 + \dfrac{r_{gs}}{R_{\text{opt}}}} \tag{14}$$

$$R_n = \frac{T_g}{T_0} r_{gs} + \frac{T_d}{T_0}\frac{g_{ds}}{g_m^2}\left(1 + \omega^2 C_{gs}^2 r_{gs}^2\right) \tag{15}$$

and

$$\text{cor} = \rho\sqrt{R_n g_n} = \frac{T_d}{T_0}\frac{g_{ds}}{g_m^2}\left(\omega^2 C_{gs}^2 r_{gs} + j\omega C_{gs}\right) \tag{16}$$

where

$$f_T = \frac{g_m}{2\pi C_{gs}}. \tag{17}$$

Although all three representations are equivalent, each of them is very useful in the subsequent discussion of theoretical and experimental results.

The expression for the available gain may be written in the form dual to that introduced in [37]:

$$\frac{1}{G_a} = \frac{1}{G_{a\max}} + \frac{g_g}{R_g}|Z_g - Z_{\text{opt}}^G|^2 \tag{18}$$

where Z_{opt}^G stands for the generator impedance realizing maximum available gain. For the equivalent circuit of an intrinsic chip (Fig. 3) $G_{a\max}$, g_g, and Z_{opt}^G are given by

$$G_{a\max} = \left(\frac{f_T}{f}\right)^2 \frac{1}{4 g_{ds} r_{gs}} \tag{19}$$

$$g_g = \left(\frac{f}{f_T}\right)^2 g_{ds} \tag{20}$$

$$Z_{\text{opt}}^G = r_{gs} + j\frac{1}{\omega C_{gs}}. \tag{21}$$

Finally, using the definition of noise measure (5) and expressions (3), (10)–(13), (18), and (19)–(21), one may search for the generator impedance Z_{opt}^M which minimizes the value of noise measure. The result is

$$X_{\text{opt}}^M = X_{\text{opt}}^G = X_{\text{opt}} = j\frac{1}{\omega C_{gs}} \tag{22}$$

$$R_{\text{opt}}^M = r_{gs}\left\{\sqrt{\left(\frac{T_g}{T_d} - 1\right)^2 + \frac{R_{\text{opt}}^2}{r_{gs}^2} - 1} - \frac{T_g}{T_d}\right\}$$

$$= r_{gs}\left\{\sqrt{\left(\frac{T_g}{T_d} - 1\right)^2 + 4G_{a\max}\frac{T_g}{T_d}} - \frac{T_g}{T_d}\right\} \tag{23}$$

where R_{opt} and $G_{a\max}$ are given by (11) and (19), respectively. The minimum value of noise measure may be obtained by substituting appropriate relations into (5).

C. Approximations and Discussion

The expressions derived in the previous section assume even simpler forms if certain conditions are satisfied. Specifically, if (compare (11))

$$\frac{f}{f_T} \ll \sqrt{\frac{T_g}{T_d}\frac{1}{r_{gs} g_{ds}}} \tag{24}$$

then

$$R_{\text{opt}} \gg r_{gs}$$

and the expressions for R_{opt} and $T_{\min}$ may be approximated by

$$R_{\text{opt}} \simeq \frac{f_T}{f}\sqrt{\frac{r_{gs}T_g}{g_{ds}T_d}} \tag{25}$$

$$T_{\min} \simeq 2\frac{f}{f_T}\sqrt{g_{ds}T_d r_{gs}T_g}\,. \tag{26}$$

Consequently,

$$\frac{4NT_0}{T_{\min}} \simeq 2. \tag{27}$$

The frequency dependence of the noise parameters given by (10), (13), (25), and (26) is the same as assumed in [23] for the purpose of the design of amplifiers at frequencies other than the frequency of measurement of noise parameters. Under this approximation, the noise parameters R_{opt}, $T_{\min}$, and g_n are functions only of f/f_T and the products $g_{ds}T_d$ and $r_{gs}T_g$, which could be considered as noise constants if values of intrinsic gate resistance and drain conductance were not precisely known.

Another interesting limiting case is for $T_g \to 0$. Then only a current noise source in the drain uncorrelated with the gate current noise source exists and

$$R_{\text{opt}} \simeq R^M_{\text{opt}} \simeq R^G_{\text{opt}} = r_{gs} \tag{28}$$

$$T_{\min} \simeq 4\left(\frac{f}{f_T}\right)^2 r_{gs}g_{ds}T_d \tag{29}$$

and

$$\frac{4NT_0}{T_{\min}} \simeq 1. \tag{30}$$

If the noise parameters of a FET (MODFET) can be described by the model, then the measured ratio of $4NT_0/T_{\min}$ must satisfy

$$1 \leqslant \frac{4NT_0}{T_{\min}} < 2 \tag{31}$$

at all frequencies. The left-hand side inequality is quite fundamental (compare (6)), while the right-hand side is a limitation of the model only (compare (14)). The parameter N is rather sensitive to measurement errors [27]; therefore, the value of $4NT_0/T_{\min}$ by itself may not always provide useful information. If, however, it is accurately known, it provides a fast check of the validity of the model and provides insight into the nature of noise sources within a transistor, without any knowledge of the transistor equivalent circuit or intervening lossless two-port (N and $T_{\min}$ are both invariant under lossless transformation at the input and/or output).

The inclusion of other elements of the equivalent circuit of a chip in this theory is straightforward, but results in rather complicated expressions. It may be viewed as a parallel and/or series and/or cascade connection of a noisy two-port of an intrinsic chip with linear passive two-ports with thermal noise source only. This can be done quite generally in a computer routine (for example, [31], [42]) using relations published in [34] and [35].

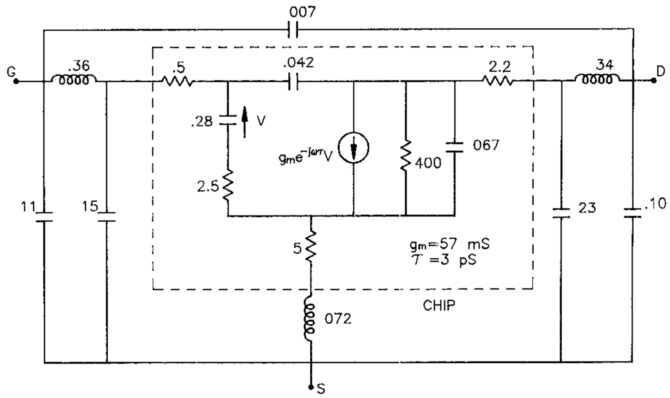


Fig. 4. Equivalent circuit of FHR01FH HEMT at $T_a = 297$ K, $V_{ds} = 2$ V, $I_{ds} = 10$ mA. Values of resistance, capacitance, and inductance are given in Ω, pF, and nH.

It is interesting to observe two invariance properties of the model upon the inclusion of source delay, τ, and drain to gate capacitance, C_{dg}.

First, it is easy to show that the inclusion of delay τ alone will not change the final expression for noise parameters $T_{\min}$, Z_{opt}, and g_n. Second, the expression for minimum noise measure $M_{\min}$ for a chip with τ and C_{dg} included will be the same as for the intrinsic chip of Fig. 3.

III. Experimental Verification

The model created in the previous section may represent, by a proper choice of constants T_g and T_d, the noise processes in the intrinsic chip which produce partially correlated noise currents at gate–source and drain–source terminals (Fig. 1(a)) with a purely imaginary correlation coefficient. The noise constants T_g and T_d need to be determined from measurement but if the equivalent circuit of a chip and its noise parameters are known, the determination is straightforward.

An equivalent circuit of a FHR01FH HEMT is shown in Fig. 4. The values of elements of the equivalent circuit were found from Fujitsu S-parameter data for both chip and packaged devices at bias $V_{ds} = 2$ V, $I_{ds} = 10$ mA [38]. The comparisons between the S parameters predicted from the model and those measured by Fujitsu for the packaged (FHR01FH) device are shown in Fig. 5. The dc characteristics and the noise parameters of the FHR01FH device (lot #C923) for room and cryogenic temperatures were given in a previous paper [23]. Although the S parameters [38] and noise parameters [23] were measured for different devices, the agreement between the measured single-stage, X-band test amplifier characteristics and those computed with the help of the equivalent circuit of Fig. 4 was excellent. As the discrepancies between measured and predicted results were about the same as differences between the measured results for different transistors from the same lot (#C923), the equivalent circuit of Fig. 4 was assumed to represent properly the transistors from that lot.

It is also interesting to point out the good agreement between the dc measured values of transconductance g_m

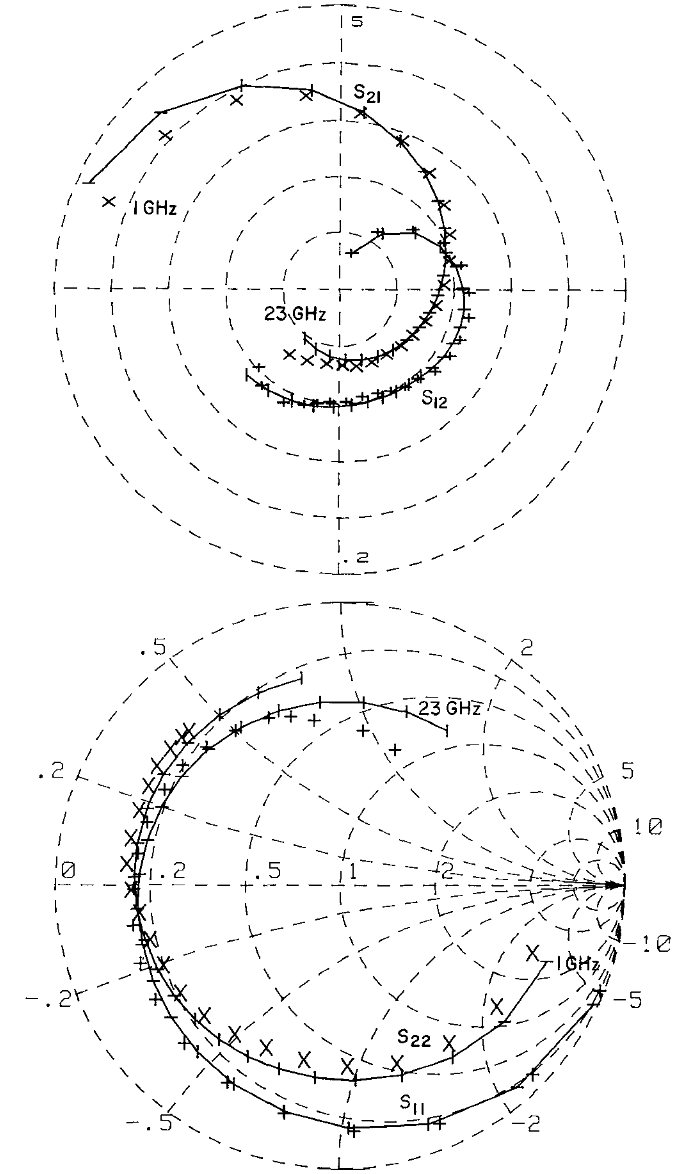


Fig. 5. Comparison between S parameters of FHR01FH measured by Fujitsu [38] and those predicted from model of Fig. 4. Lines with ticks are for computed data while crosses indicate measured points.

and source-to-drain resistance $r_{ds} = 1/g_{ds}$ [23] with those determined from S parameters [38]. Usually, for GaAs FET's the value of r_{ds} determined from microwave measurements is smaller than the dc measured value by a factor of about 2 or more [39]–[41]. This phenomenon has been linked to the existence of traps in GaAs and/or at the interface between active and buffer layers [39], [41]. The absence of this phenomenon in the case of the FHR01FH HEMT points to a very low trap density. The excellent noise performance of the FHR01FH and its relative insensitivity to an illumination at cryogenic temperatures [23] corroborate this observation.

A knowledge of the equivalent circuit and the noise parameters of the packaged device and its physical temperature allows the determination of the noise parameters of an intrinsic chip. This process, known as de-embedding, may be done with the help of the general relations from [34] and [35], which lend themselves naturally to computer implementation [31], [42].

The values of noise parameters of a FHR01FH transistor at different stages of de-embedding are tabulated in Table I. The data for the packaged device in the first row of Table I are the same as those published in [23]. The data in subsequent rows were obtained by removing the influence of the package parasitics (second row), the gate, drain, and source parasitic resistances (third row), and finally the source-to-drain capacitance (fourth row). For room temperature the elements of the equivalent circuit of Fig. 4 were used. For cryogenic temperature the transconductance, g_m, and drain-to-source resistance, r_{ds}, were changed to 50 mS and 500 Ω, respectively. These values were obtained by multiplying the respective values of g_m and r_{ds} from Fig. 4 by the ratios determined from the measurement of their dc counterparts [23, fig. 6].

The values of the noise parameters from the last row of Table I may now be compared with those resulting from expressions (10)–(13) of Section I for the best fit of equivalent temperatures T_g and T_d. This is done in Table II. First, the consistency of the model may be verified by comparing the values of optimal source reactance, as both values were arrived at independently. One is derived from measured noise parameters [23] de-embedded from the influence of the packaged HEMT parasitics; the other is simply $1/\omega C_{gs}$. The agreement is indeed remarkable, well within the range of estimated accuracy of noise parameter measurements [23]. The remaining three noise parameters, $T_{\min}$, R_{opt}, and g_n, of the model were determined by finding T_g and T_d which by the use of (11)–(13) provided the best fit in the mean square sense to the de-embedded measured noise parameters.

For the purpose of the discussion to follow in Section III, the process of de-embedding and fitting of T_g and T_d was repeated for $r_{gs} = 3.5$ Ω and the results are also included in Table II.

A knowledge of the equivalent temperatures T_d and T_g and the elements of the equivalent circuit at a given ambient temperature T_a allows the computation of noise parameters at any frequency. The computed results for a FHR01FH device (packaged) and a FHR01X device (chip) at 297 K and 12.5 K are shown in Figs. 6, 7, 8, and 9, respectively. They are also compared with available experimental results.

For the packaged device, the experimental results at 8.5 GHz are those of Table I (first row) and previously published in [23]. The cryogenic results at 4.8 GHz and 10.7 GHz are derived from multistage amplifier measurements also reported in [23]. The room-temperature and cryogenic results at 15 GHz are reported in [43]. The room-temperature data for $T_{\min}$ and G_{as} from the FHR01FH (packaged) data sheet [38] are also included. Analysis of noise parameters data of the FHR01FH published by Fujitsu [38] for the frequency range 4–20 GHz reveals good agreement for

TABLE I
NOISE PARAMETERS OF FHR01FH AT DIFFERENT STAGES OF DE-EMBEDDING ($f = 8.5$ GHz, $V_{ds} = 2$ V)

	T_a = 297 K, I_{ds} = 10 mA				T_a = 12.5 K, I_{ds} = 5 mA			
NOISE PARAMETERS	T_{min} K	R_{opt} Ω	X_{opt} Ω	g_n mS	T_{min} K	R_{opt} Ω	X_{opt} Ω	g_n mS
PACKAGED FET	78.0	10.5	17.5	9.4	10.0	4.4	17.0	2.6
FET CHIP	79.1	26.3	53.8	3.8	10.1	11.2	57.2	1.0
INTRINSIC CHIP WITH C_{gd}	64.6	20.7	53.7	3.8	8.1	8.8	57.2	1.0
INTRINSIC CHIP WITHOUT C_{gd}	65.6	26.3	59.5	3.0	8.2	11.4	65.2	.80

TABLE II
COMPARISONS OF NOISE PARAMETERS OF FHR01 INTRINSIC CHIP ($f = 8.5$ GHz)

T_a K	Comments	T_{min} K	R_{opt} Ω	X_{opt} Ω	g_n mS	T_g K	T_d K
297	From Table I	65.6	26.3	59.5	3.0	-	-
	Model Best Fit for r_{gs} = 2.5 Ω	58.7	28.4	66.9	3.27	304	5514
	Model Best Fit for r_{gs} = 3.5 Ω	59.6	28.2	66.9	3.24	210	5468
12.5	From Table I	8.2	11.4	65.2	.80	-	-
	Model Best Fit for r_{gs} = 2.5 Ω	7.4	12.3	66.9	.87	14.5	1406
	Model Best Fit for r_{gs} = 3.5 Ω	7.7	12.0	66.9	.85	9.3	1379

T_{min} and G_{as}, excellent agreement for X_{opt}, and relatively poor agreement for R_{opt} and g_n. The FHR01FH Fujitsu data should, however, be viewed with caution as the invariant parameter $4NT_0$ computed from these data for the frequencies 18 GHz and 20 GHz falls below the value of T_{min}, thus violating the fundamental inequality (6).

To the contrary, the Fujitsu noise data for the FHR01X (chip) [38] from 4 to 20 GHz show good agreement with the prediction of the model, as is demonstrated in Fig. 7. The model data in Fig. 7(a) are for the chip as outlined by a broken line in Fig. 5 and were determined from the noise parameter measurement of a single packaged device at 8.5 GHz [23], representing well the devices from lot #C923. The model data of Fig. 7(b) are for the same chip with parasitic inductances added ($L_g = 0.12$ nH and $L_s = 0.07$ nH) and drain temperature T_d recomputed to provide the best fit to Fujitsu measured data under the assumption $T_g = T_a = 297$ K. It is not known if the Fujitsu chip data are a representation of measurements of many samples or a single sample measurement data. In any case, an agreement between measured and predicted values of noise parameters is excellent. The only experimental point in

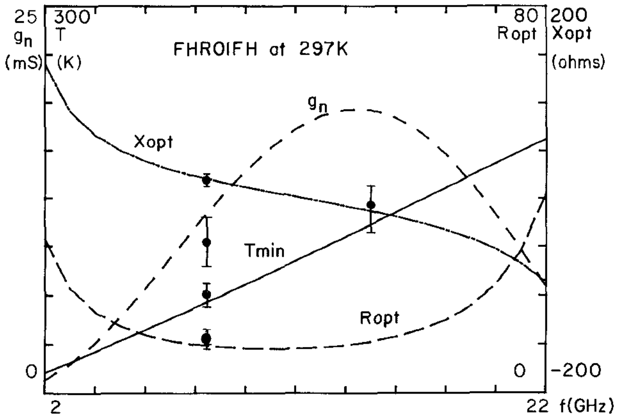


Fig. 6. Noise parameters of FHR01FH HEMT at $T_a = 297$ K and $V_{ds} = 2$ V, $I_{ds} = 10$ mA. Lines indicate data obtained from the model using the equivalent circuit of Fig. 4; $T_g = 304$ K and $T_d = 5514$ K. Points indicate data from [23] and [43].

Fig. 9 for the cryogenic FHR01X (chip) is derived from the amplifier measurement reported in [23].

IV. Discussion of Results

A very interesting question to pose is what physical significance, if any, should be attached to the values of gate and drain equivalent temperatures, T_g and T_d. Clearly, T_d is an equivalent temperature of the output impedance of a FET if the gate at the chip terminal is open-circuited. The value of several thousand K at room temperature (compare Table II and Fig. 7) is very consistent with recently published results of equivalent noise temperatures of "resistor-like" AlGaAs–GaAs structures [44]. The values in excess of 1000 K were measured for an average electric field intensity of about 4×10^3 V/cm. If the data were extrapolated to the value of a field intensity of about 10^4 V/cm (2 V across 2 μm gate-to-drain separation of a FHR01 HEMT), the values of the equivalent noise temperatures would be in the range of several thousand kelvins. This quantitative agreement between different wafer and device structures [44], [45] encourages the interpretation of drain equivalent temperature as a physical parameter and not merely a fitting factor in a model.

An interpretation of the gate equivalent temperature as a physical temperature of resistance r_{gs} poses greater difficulty. As is clear from the derivation of noise parameter expressions, an assignment of an equivalent gate temperature to the intrinsic gate resistance can model any noise process within a FET which produces perfectly correlated short-circuit noise currents at the input and output with a purely imaginary correlation coefficient. However, any noise-generating mechanism postulated by other methods of analysis [1]–[11] will produce current noise sources at intrinsic chip terminals which can always be split into a pair of perfectly correlated current noise sources with a purely imaginary correlation coefficient at the gate and drain terminals and a single uncorrelated current noise source at the drain terminal. Thus, random variations of a depletion layer boundary (channel "breathing" [5]), random variation of a quantum well width, random variation of the sheet density of 2 DEG, etc., may all be viewed as an application of a voltage noise generator in series with a depletion layer capacitance. If r_{gs} correctly models the resistance through which the depletion layer capacitance is charged or discharged, then this noise source may be modeled by an assignment of a certain temperature T_g to the resistance r_{gs}.

It is a well-known fact that an accurate determination of r_{gs} is very difficult [41]. The value of r_{gs} in any S-fitting algorithm may be easily traded for values of parasitic resistance r_g, and/or parasitic resistance r_s [41], and/or transconductance g_m and parasitic source inductance L_s [47]. Even the value of the sum of r_{gs}, r_g, and r_s may not be precisely determined. For example, the S-parameter data for the FHR01FH of Fig. 4 could be fitted well within the measurement error by the circuit model of Fig. 4 but with $r_{gs} = 3.5$ Ω. Repeating the process of de-embedding and fitting for this modified circuit results in as good a fit of noise parameters, but for markedly different values of T_g (compare Table II). In view of the discussion from Section II, this is not surprising, as the noise parameters are a function of the products $r_{gs}T_g$ and $g_{ds}T_d$. Whether T_g may be treated as a fitting factor or a parameter with a physical meaning is, therefore, determined by how accurately the value of r_{gs} is known.

The values of T_g in Table II for $r_{gs} = 2.5$ Ω are about equal to the ambient temperature. By changing the value of r_{gs} within the measurement error, the best fit value of T_g can be made either larger or smaller. However, upon cooling the value of T_g decreases in proportion to the ambient temperature, while the value of T_d does not (compare Table II). This observation strongly suggests that the source of noise producing perfectly correlated noise currents at gate and drain terminals is inherently thermal in origin. If this observation is correct, an upper bound could be established for r_{gs}. For example, in the case of the FHR01FH HEMT, $r_{gs} \leqslant 2.5$ Ω, as the values of $r_{gs} > 2.5$ Ω result in best fit values of T_g which are smaller than ambient temperature T_a (Table II).

More experimental data need to be gathered and analyzed to confirm or deny the assertion of the thermal origin of the noise source producing perfectly correlated noise currents at the gate and drain. It is recognized, however, that there exists an anisotropy in electron dynamics in a HEMT channel, as the diffusion coefficient D is not only field dependent but also very different in directions perpendicular and parallel to the interface [10]. By analogy the parameters T_g and T_d could be interpreted as electron temperatures averaged over the length of the channel in directions perpendicular and parallel to the channel, respectively. Thus, electron heating by the electric field would be negligible in the direction perpendicular to the channel, resulting in T_g values being close to the ambient temperature.

V. Comparison with Other Methods

The most elegant and detailed theory of noise properties of a MESFET is that of Pucel, Haus, and Statz [5]. Many

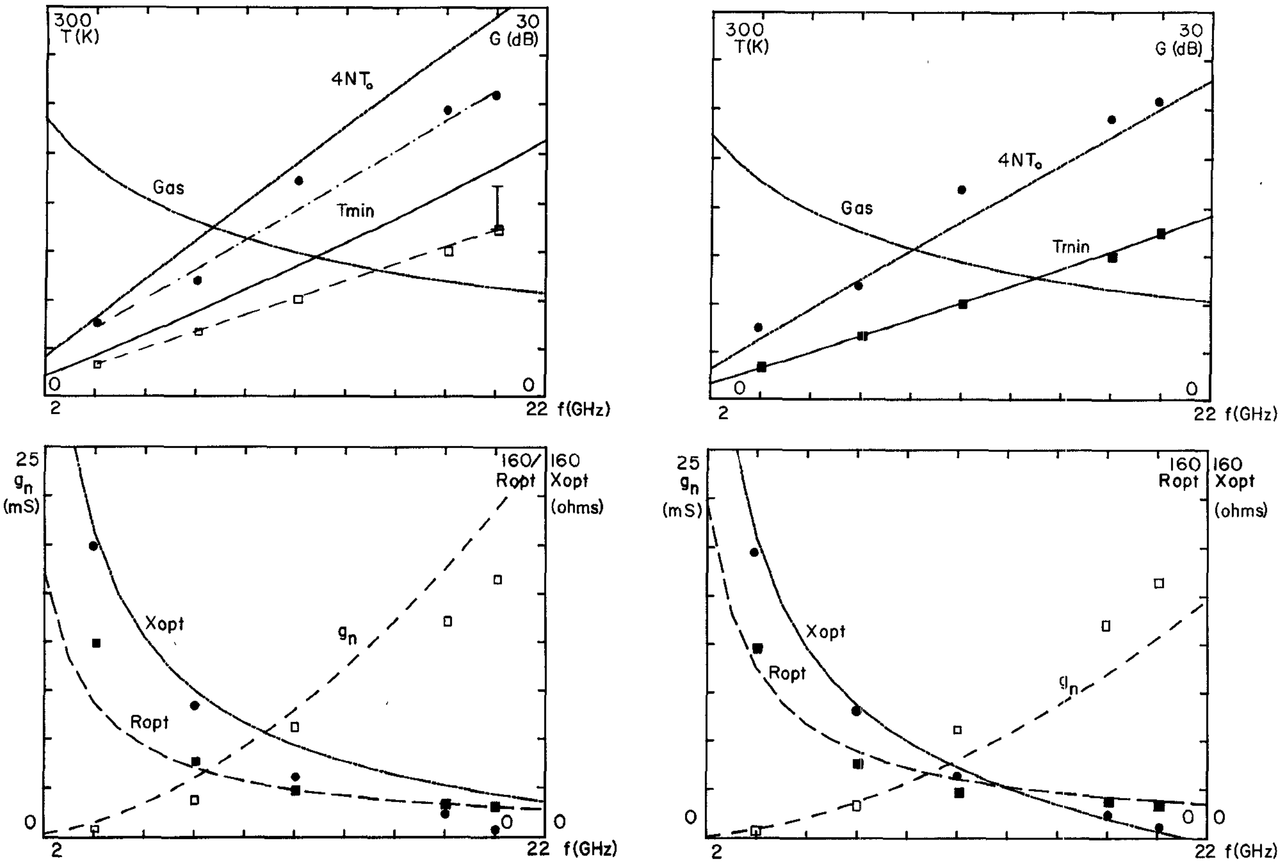


Fig. 7. Comparison of noise parameters of FHR01X (chip) HEMT at room temperature computed from the model with experimental results from Fujitsu data sheet [38]. For computations, a part of the equivalent circuit of Fig. 4, denoted by broken lines with source inductance added, was used. (a) For the model data $T_g = 304$ K, $T_d = 5514$ K, $T_a = 297$ K were used. T_g and T_d were determined from a single noise parameter measurement of a package device (lot #C923) at 8.5 GHz. (b) For the model data $T_g = T_a = 297$ K was assumed and $T_d = 3364$ K was found to fit best Fujitsu measured data. Also, the equivalent circuit of a chip was amended with parasitic gate inductance $L_g = 0.12$ nH. See text for additional comments.

later papers [7]–[10], [13] draw heavily on ideas presented in [5] as reviewed in a recent paper by Cappy [20].

Under a small frequency approximation, the expressions (10), (13), (25), and (26) are equivalent to [5, eq. (95), p. 248] or [20, eqs. (17)–(19)] if

$$K_g = \frac{g_{ds}}{g_m}\frac{T_d}{T_0} \tag{32}$$

$$K_r = g_m r_{gs}\frac{T_g}{T_0} \tag{33}$$

$$K_c = 1 \tag{34}$$

where K_g, K_r, and K_c are the dimensionless noise coefficients defined in [5].

This demonstrates that if (34) is not satisfied as called for in [5], the only difference in the noise parameter expression under small frequency approximations will be in X_{opt} because [5], [20]

$$X_{\text{opt}} = \frac{K_c}{\omega C_{gs}}. \tag{35}$$

The experimental data of Section II and other experiments [40] show K_c to be equal to unity within an experimental

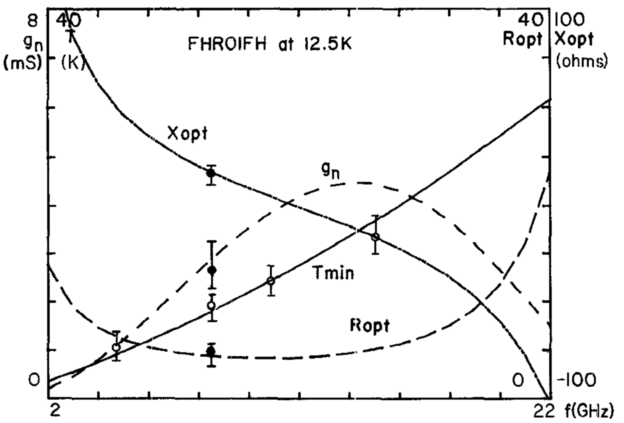
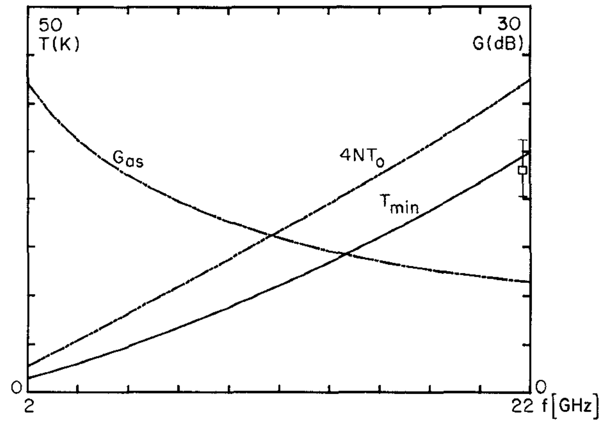


Fig. 8. Noise parameters of FHR01FH HEMT at $T_a = 12.5$ K and $V_{ds} = 2$ V, $I_{ds} = 5$ mA. Lines indicate the data obtained from the model using equivalent circuit of Fig 4, $g_m = 50$ mS, $r_{ds} = 500$ Ω, $T_g = 14.5$ K, and $T_d = 1406$ K. Points indicate experimental data from [23] and [43].

uncertainty. The example of Monte Carlo simulation presented in [20, fig. 5] gives $K_c = 1.25$. The values of K_c of about 2 or more given in [5, figs. 23 and 24] should therefore be treated with caution. A qualitative explanation of this discrepancy is quite simple. The correlation coefficient C in [5] is computed assuming that the modula-



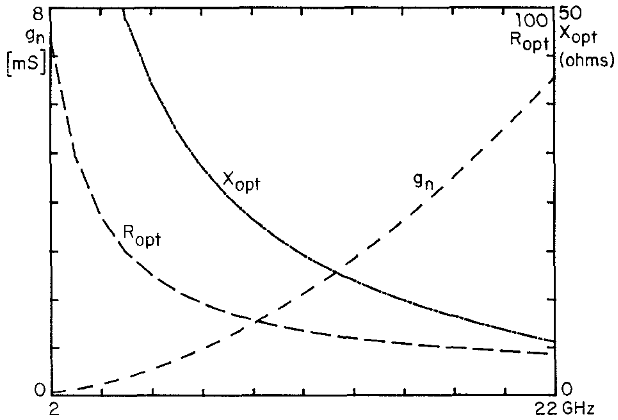


Fig. 9. Noise parameters of FHR01X (chip) HEMT at $T_a = 12.5$ K. For computations, a part of the equivalent circuit of Fig. 4, denoted by broken lines with source inductance added, was used with $g_m = 50$ mS, $r_{ds} = 500\ \Omega$, $T_g = 14.5$ K, and $T_d = 1406$ K. The experimental point at 22 GHz is determined from noise temperature measurement of multistage amplifier [23].

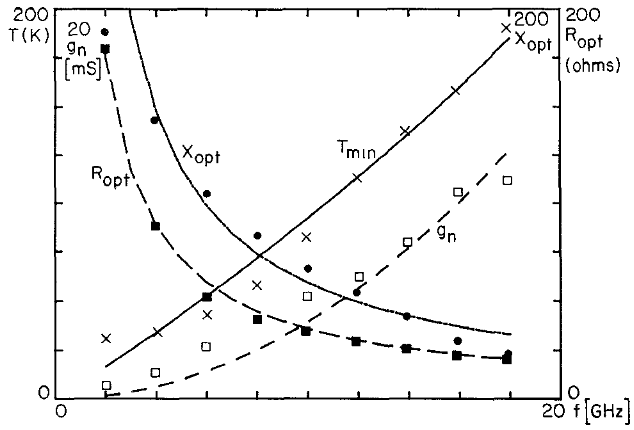


Fig. 10. Comparison between data for NE045 chip given by Gupta and Greiling [19, table I] and the present model. Under the assumption $T_g = 296$ K, $r_{ds} = 450\ \Omega$, and $g_m = 36.5$ mS, the values of R_T and T_d were best fitted using model expression for T_{min}, R_{opt}, and g_n. The values of C_{gs} was best fitted using the expression for X_{opt}. These best fit values are $R_T = 4.8\ \Omega$, $C_{gs} = 0.27$ pF, and $T_d = 2374$ K. See text for additional comments

tion of charge due to random drain current variations occurs only in the "active" part of the depletion layer, while gate-to-source capacitance is computed for the whole depletion layer including edge effects [5, eq. (33), p. 221]. However, in any small-signal model of a FET, the C_{gs}, across which the voltage controlling a current source is built, should represent only an "active" part of the depletion layer; the remaining capacitance should be a part of an embedding circuit.

While under the small-signal approximation the model of Pucel *et al.* [5] and its extensions and improvements [20] are "nearly" equivalent in a formal sense to the model of Section II, they reveal a different physical picture of noise phenomena. If the gate noise current of an intrinsic chip were indeed induced by the drain current fluctuations, then the rate of decrease of T_d and T_g upon cooling should be about the same. The data of Table II do not confirm this observation, as discussed in Section IV. More accurate experimental data should resolve this discrepancy as well as that of the expression for X_{opt}.

Recent work by Gupta *et al.* [18], [19] claims that the noise parameters over a wide frequency range may be predicted from a single output noise power measurement at low frequency and a knowledge of the elements of a FET equivalent circuit. The important assumption of their analysis [18] is that R_T (which includes r_{gs}) is at temperature $T_g = 290$ K. In our model the best fit of measured noise parameters of a FHR01FH indeed results in the equivalent gate temperature T_g quite close to the ambient temperature T_a. The discussion of Section IV, however, indicates that this *a priori* assumption may corrupt the accuracy of noise parameter prediction if an error in estimation of r_{gs} and, therefore, R_T is present (compare data of Table II). As an illustration, the data for the NE045 chip [19, table I] were transformed into a set of noise parameters T_{min}, Z_{opt}, and g_n. T_d and R_T were then fitted under the assumption $T_g = T_a = 296$ K. The results are presented in Fig. 10. The maximum deviation of measured NE045 chip noise temperature and model prediction for $R_T = 4.8\ \Omega$ (see Fig. 10) is only 13 K as compared with 26 K [19, fig. 2] for Gupta's model, in which $R_T = 7.1\ \Omega$ [19, table II]. On the other hand, if $R_T = 7.1\ \Omega$, then as good a fit to the measured noise parameters would require $T_g = 200$ K.

One more comparison of the results of Section III can be made with those of a recent paper by Oxley and Holden [16]. They find experimentally that the noise figure and its departure from linear frequency dependence are a strong function of gate width for otherwise identical devices. They explain this in terms of a distributed model of a FET, finding that the departure from a linear dependence occurs at the frequency at which the gate width is about 1/20 of an average wavelength of the first two lowest order propagation modes. This frequency in their data could be as low as 20 GHz for a 100-μm-gate-width, 0.3-μm-gate-length device [16, fig. 7]. To the contrary, a recent theoretical study [46] predicts no significant difference between a lumped-element model and a distributed model for a 100 μm, 0.25 μm device for up to 50 GHz. In our model a significant departure from a linear dependence of noise temperature on frequency will occur at about

$$f_c \simeq \frac{g_m}{2\pi C_{gs}} \sqrt{\frac{T_g}{T_d} \frac{1}{r_{gs} g_{ds}}} \tag{36}$$

which follows directly from inequality (24). This is confirmed by experimental data for the FHR01FH HEMT (which is 200 μm wide) of Section III, indicating an absence of distributed type effects for the device up to 22 GHz. The experimental data of [16] can, however, be qualitatively explained by a wafer nonuniformity. Both $T_{\min}$ for $f \ll f_c$ (eq. (26)) and f_c (eq. (36)) will remain invariant upon a change in the gate width if the values of the ratio g_m/C_{gs}, the product $r_{gs} g_{ds}$, and equivalent temperatures T_g and T_d remain invariant under the condition of a constant current per unit gate width. The presence of nonuniformities at the interface between active and buffer layers and/or variations in epilayer thickness will affect the values of g_m [7], g_{ds}, and T_d much more than those of C_{gs}, r_{gs}, and T_g. In this case, for an increasing gate width, the ratio g_m/C_{gs} is likely to go down while the product $g_{ds} r_{gs}$ and T_d are likely to go up. That is, $T_{\min}$ increases (eq. (30)) and f_c decreases (eq. (36)), providing a qualitative explanation of the experimental data of [16].

VI. Conclusions

This paper presented a novel approach to the modeling of noise behavior of FET's and MODFET's over a wide frequency range. A simple closed-form expression for minimum noise temperature $T_{\min}$, optimal source impedance Z_{opt}, noise conductance g_n, and source impedance $Z^M_{g\text{opt}}$ minimizing noise measure was derived. These were found to be functions of the elements of a small-signal equivalent circuit of a FET and two frequency-independent constants, named equivalent gate and drain temperatures. The equivalent temperatures in the example of a FHR01FH MODFET were demonstrated to be independent of frequency in the frequency range in which $1/f$ noise is negligible. Thus, the model allows prediction of noise parameters over a broad frequency range from a single frequency noise parameter measurement. The same example of a FHR01FH MODFET presents a different physical picture of the source of the gate noise in MODFET's than that usually accepted, showing it to be of thermal origin only. More accurate experiments for both FET's and MODFET's should resolve this question. The equivalence relations and/or conditions between this approach and other relevant studies were established. The model uses only circuit theory concepts and therefore is very easy to implement in any CAD and/or CAM package. Finally, it is hoped that it may be used by device manufacturers as a standard noise description of commercial devices.

Acknowledgment

The author would like to thank Dr. S. Weinreb for his helpful comments. Also, the excellent experimental and technical assistance of W. Lakatosh is greatly appreciated.

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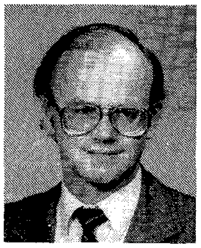

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